Advanced Si and SiGe Strained Channel NMOS and PMOS Transistors with High-K/Metal-Gate Stack

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Abstract. Sustaining Moore's Law of scaling Si CMOS transistors will require not only shrinking the transistor dimensions, but also introduction of new materials and structures. In the future, advanced high performance CMOS transistors are likely to incorporate highly strained Si and SiGe channel for enhanced carrier transport and high-K/metal-gate stack for low gate leakage. This work describes the recent advances made in integrating strained Si and SiGe channel transistors with high-k/metal-gate stack for future high performance, low power logic applications.

I. INTRODUCTION

The silicon industry has been aggressively scaling the physical thickness of the gate oxide, which is silicon dioxide (SiO2), along with the transistor physical gate length for more than 15 years for high performance CMOS applications. Recently, SiO2 with physical thickness of only 1.2 nm has been successfully implemented in Intel's 90nm logic technology node, which is currently in production [1]. This technology node also witnessed a major material change in the use of epitaxial SiGe (silicon germanium) as source-drain regions in PMOS transistors to incorporate significant levels of strain into the Si channel for hole mobility enhancement [2]. In the future, continual gate stack scaling will require alternate dielectric with higher dielectric constant (K) and larger physical thickness, since a) the gate leakage due to quantum mechanical tunneling of electrons/holes is increasing exponentially with reducing SiO2 thickness and b) SiO2 is literally running out of atoms to scale. Hafnium dioxide (HfO2) is considered as one of the most promising high-K candidates to replace SiO2 in future generations of CMOS transistors due to its sufficiently large band offsets, thermodynamic stability in contact with Si [3] and excellent high frequency response [4]. However, the most serious drawback in integrating HfO2 in high performance CMOS technology is the 40-50% degradation in electron mobility with HfO2/poly-Silicon gate stack [5]. In our research lab, we have successfully fabricated NMOS transistors incorporating significantly high levels of strain by integrating a biaxial tensile strained Si channel on relaxed SiGe virtual substrate, HfO2 gate dielectric and TiN (titanium nitride) metal-gate electrode, to enhance electron mobility even beyond the SiO2 universal mobility curve [6]. To enhance hole mobility, we have successfully fabricated PMOS transistors using a biaxial compressively strained SiGe channel and HfO2 gate dielectric and TiN metal-gate stack, to demonstrate hole mobility higher than the SiO2 universal mobility curve [7]. These experimental results are encouraging and show that, high-K/metal-gate stack, in conjunction with strained Si and SiGe channels, can be implemented in future generations of advanced CMOS devices for low power, high performance logic and RF applications.

II. TENSILE STRAINED SILICON NMOS

Figure 1 shows a schematic illustration of the NMOS device structure fabricated. A thin layer of tensile strained Si is deposited on a 1.5 um thick layer of compositionally graded and fully relaxed SiGe (Ge=10-19%) by UHVCVD process, followed by HfO2/TiN metal-gate deposition and device fabrication. The higher the Ge concentration, the higher is the strain in the Si channel. Control devices were also fabricated on conventional unstrained Si substrate with HfO2/TiN gate stack. Figure 2 shows the cross-sectional TEM image of the tensile strained Si channel layer on the relaxed SiGe virtual substrate. Figure 3 shows that, for the same electrical equivalent oxide thickness (EOT), more than 1000 times reduction in gate leakage is achieved in HfO2/TiN gate on both strained and unstrained Si, compared to the SiO2/poly-Silicon control. Effective inversion electron mobility was measured on long channel

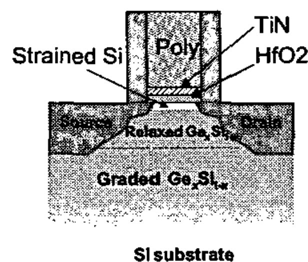

Figure 1. A schematic of strained Si NMOS transistor with HfO2/TiN metal-gate stack.

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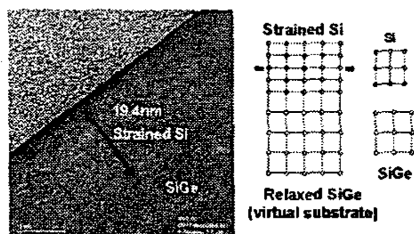

Figure 2. Biaxial tensile strained silicon layer on relaxed SiGe virtual substrate for NMOS application.

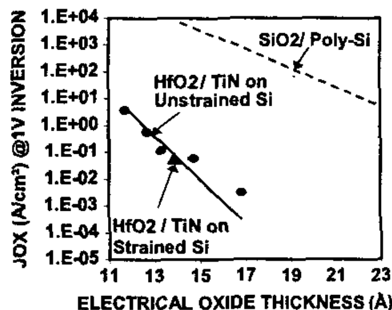

Figure 3. Gate leakage as a function of electrical oxide thickness measured in inversion for HfO2/TiN metal-gate stack. Also shown is SiO2/poly-Silicon line for reference. Difference in slopes is due to the conduction band offset between HfO2 (~1.5eV) vs SiO2 (~3.0eV).

devices at low drain bias as a function of the vertical electric field in the channel (Eeff), as shown in Figure 4. Devices with HfO2/poly-Silicon gate stack show significant degradation in electron mobility compared to SiO2/poly-Silicon devices. HfO2/TiN metal gate stack recovers a majority of the degradation to close to the SiO2/poly-Silicon level and biaxial tensile strain in Si (10% and 15% Ge virtual substrate) provides additional mobility enhancement. To analyze and understand the physics of the electron mobility improvement mechanism with TiN metal gate

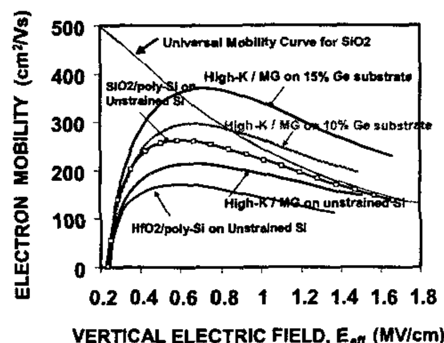

Figure 4. Channel electron mobility of HfO2/TiN gate stacks on tensile strained Si with 10% and 15% Ge in the SiGe layer. Also shown is HfO2/poly-Si on unstrained Si.

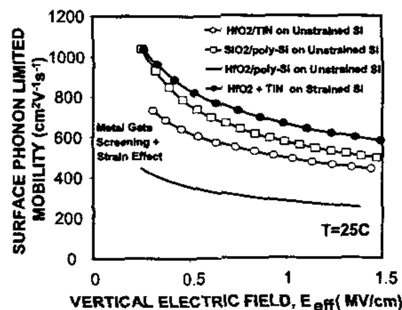

Figure 5. The use of metal gate and strained Si is effective in screening the interaction between high-K remote phonons and channel electrons and improves the surface phonon limited mobility.

electrode and strained Si channel, we measured the mobility as a function of temperature and Eeff, and extracted the surface phonon limited mobility using an inverse modeling technique [8] .Figure 5 shows that, the devices with HfO2/poly-Silicon gate stack suffer from a severe surface phonon induced degradation mechanism, and that both metal gate and strained Si channel help improve the surface phonon limited mobility. This additional surface phonon induced degradation in high-K/poly-Silicon gate stacks is believed to be caused by the coupling of low energy surface optical (SO) phonon modes arising from the polarization of the high-K to the inversion channel electrons [9]. For a given high-K thickness, we believe, that the TiN metal gate with higher free electron density is more effective in screening the interaction between the remote high-K optical phonons and the channel electrons under inversion conditions, whereas the depleted poly-Si gate electrode with lower free electron density is less effective [8,9]. Biaxial tensile strain in Si further enhances the surface phonon limited mobility. This improvement results from two effects: a) reduction in the transport mass from the energy lowering and the resulting repopulation of the two out-of-plane

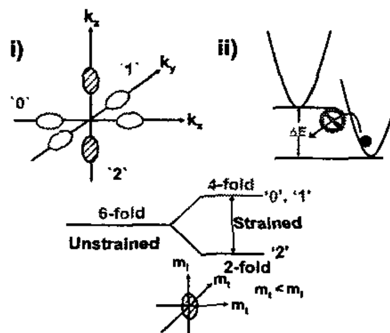

Figure 6. Biaxial tensile strain causes energy splitting of the six-fold degenerate conduction band valleys causing preferential occupation of the out-of-plane valley '2' which has lower in-plane effective mass and also reduces inter-valley scattering.

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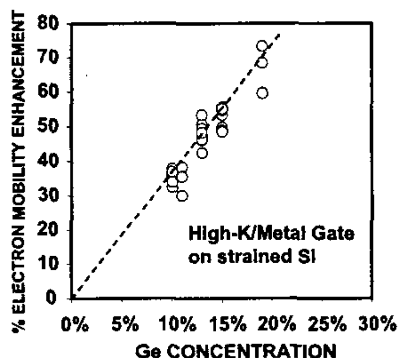

Figure 7. Electron mobility enhancement factor in percentage with biaxial tensile strained Si with HfO2/TiN metal-gate stack plotted vs Ge concentration in the SiGe virtual substrate.

conduction valleys with lower in-plane mass, and also b) reduction in inter-valley phonon scattering from the energy splitting of the conduction band valleys due to strain (Figure 6) [10]. Figure 7 plots the high field (1MV/cm) electron mobility enhancement in percentage from biaxial tensile strain in NMOS transistors with high-K/metal-gate stack as function of the Ge concentration. Biaxial tensile strained Si can provide as high as 75% enhancement in long channel electron mobility with high-k/metal-gate stack making it a promising NMOS device technology for future high performance logic applications.

III. COMPRESSIVELY STRAINED SILICON-GERMANIUM PMOS

The use of biaxial tensile strain is not as effective in enhancing the hole mobility for PMOS applications because the mobility gain observed at low vertical field reduces at high vertical electric field [11,12]. This is attributed to the fact that, unlike uniaxial compressive strain [13] which redistributes holes to the in-plane wings with the lowest effective mass along current direction <110>, the biaxial tensile strain enhances hole mobility at low field primarily due to inter-band scattering suppression resulting from light and heavy hole band splitting which quickly drops off at high vertical field due to 2D surface confinement effects [14,15]. Figure 8 shows the schematic and TEM cross-section of a PMOS transistor structure where a biaxial compressively strained SiGe layer is formed on top of the silicon substrate. No dislocation defects within the SiGe film are seen across the channel region. High-K/TiN metal-gate was deposited directly on the compressive SiGe channel layer, followed by transistor fabrication steps. Figure 9 shows that the PMOS hole mobility enhancement induced by the biaxial compressive strain in the SiGe layer increases with increasing Ge %, and that this hole mobility gain does not reduce at high vertical electric field in the channel as in the case of the biaxial tensile strained Si case. The biaxial

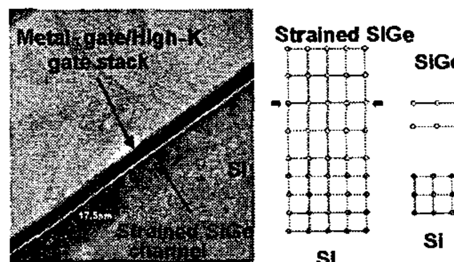

Figure 8. Biaxial compressively strained SiGe layer formed on top of a Si substrate upon which surface channel PMOS transistors are fabricated.

compressive strain in the SiGe layer lifts the light and heavy hole degeneracy, making heavy hole band more light hole like, thereby enhancing hole mobility mobility through effective mass reduction and inter-band scattering suppression, as qualitatively illustrated in Figure 10.

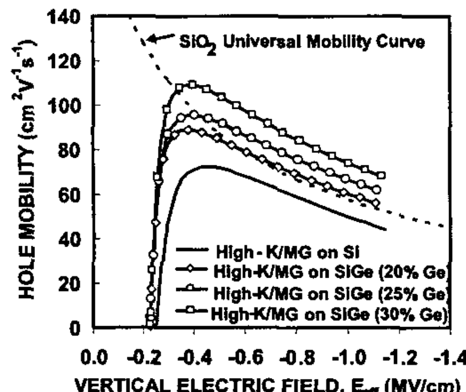

Figure 9. PMOS hole mobility gain induced by biaxial compressive strain in the SiGe channel increases with increasing Ge % in the SiGe layer. This mobility gain does not reduce at high vertical Eeff like in the case of biaxial tensile strain in Si.

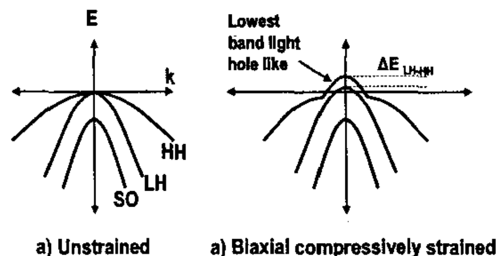

Figure 10. Simplified in-plane valence band energy vs k diagram for unstrained and biaxial compressive strained SiGe. Energy splitting between light and heavy holes causes band-mixing resulting in repopulation to the light-hole like band improving transport mass and also reducing inter-band scattering.

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Due to the valence band discontinuity (ΔEv) between SiGe channel and Si substrate, PMOS devices on compressively strained SiGe have lower Vt than the Si devices as shown in the inversion split C-V measurements, making an otherwise mid-gap (on silicon) TiN electrode a suitable metal gate electrode (Figure 11) for PMOS applications. Recently, more than 2X improvement in hole mobility with very high concentration of Ge (80% and 100%) have been reported [16,17], making compressively strained SiGe or Ge channel PMOS transistors another promising emerging device technology.

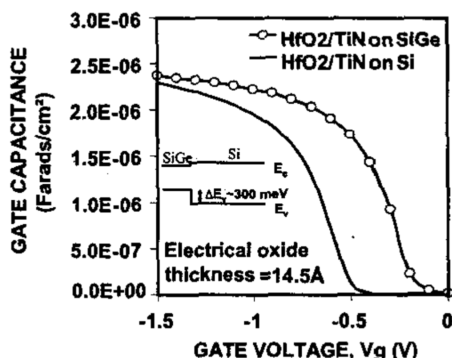

Figure 11. Split C-V characteristics of HfO2/TiN metal gate stack showing 14.5A electrical oxide thickness in inversion on both unstrained Si and strained SiGe transistors with 0.3V threshold voltage difference arising from valence band offset.

IV. SUMMARY

This paper summarizes the recent advances in integrating biaxial tensile strained Si and compressively strained SiGe channel NMOS and PMOS transistors with high-K/metal-gate stack. It is shown that up to 75% improvement in electron mobility in long channel NMOS transistors can be achieved with biaxial tensile strained Si on relaxed SiGe substrate. On the PMOS side, it is shown that compressively strained SiGe channel may be used in enhancing hole mobility by 55% at high vertical Eeff, which cannot be achieved with biaxial tensile strain. Through new materials introduction in the transistor structure and by incorporating significantly higher levels of strain in the channel, it is expected that high performance CMOS transistor scaling and Moore's Law will continue in the near future.

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